CLAIMS

1. An active matrix display, comprising:

an array of pixels provided over a common substrate, each pixel comprising a display element (16) and a switching device (14); and

a column driver (32) for providing signals to the pixels for driving the display elements, the column driver comprising digital to analogue converter circuitry and providing a first number of display element drive levels greater than 2,

wherein each pixel comprises means for converting the first number of display element drive levels into a second, greater number, of pixel grey levels.

2. A display as claimed in claim 1, wherein the means for converting comprises, within each pixel, at least first and second display elements (40,42) having different areas.

3. A display as claimed in claim 2, wherein the first and second display elements (40,42) have areas in the ratio 1:2.

4. A display as claimed in claim 1, wherein the means for converting comprises, within each pixel, charge redistribution circuit elements (S1, S2, 16a, 16b).

5. A display as claimed in claim 4, wherein the charge redistribution elements comprise two display elements (165a, 16b), an input switch (S1) between the input to the pixel and a first display element (16a) and a charge redistribution switch between the first and second display elements (16a, 16b).

6. A display as claimed in any preceding claim, wherein the digital to analogue circuitry receives a 5 bit digital word.

7. A display as claimed in claim 6, wherein the output of the digital to analogue circuitry comprises a number of levels less than 32.

8. A display as claimed in claim 7, wherein the output digital to analogue circuitry comprises 22 possible levels.

9. A display as claimed in any preceding claim, further comprising a converter for deriving from a 6 bit drive signal a signal for selecting which one or ones of the first number of levels to apply to each display element.

10. A display as claimed in claim 9, wherein the converter comprises a divider for dividing by 3 and providing a divisor and a remainder.

11. A display as claimed in claim 10 and claim 2, wherein the divisor determines which of the first number of levels is applied to one or both of the display elements (40,42), and the remainder determines which one or ones of the display elements this determined level is applied to.

12. A display as claimed in claim 11, wherein an adjacent level is applied to the display elements (if any) to which the determined level is not applied.

13. A display as claimed in any preceding claim, comprising a plurality of row conductors (10), a number of row conductors (10a, 10b) being associated with each row of pixels corresponding to the number of display elements (40,42) within each pixel.

14. A display as claimed in any preceding claim, wherein each pixel comprises a memory element (52) for storing digital drive values for the display elements of each pixel.

15. A display as claimed in any preceding claim, wherein the digital to analogue circuitry is provided on the common substrate.

16. A display as claimed in claim 15, wherein the pixel array and the digital to analogue circuitry are formed using low temperature polysilicon processing.

17. A method of driving an active matrix display, comprising:

providing first and second drive voltages to a display pixel having first and second display elements (40,42; 16a,16b), the first and second drive voltages being selected from two adjacent drive voltage levels of a digital to analogue converter which has more than 2 output levels; and

within the pixel, generating an intermediate grey level corresponding to a drive voltage between the first and second levels.

18. A method as claimed in claim 17, wherein the first display element (40) has a first area and the second display element (42) has a second area different to the first area, area weighting being used to generate the intermediate grey level.

19. A method as claimed in claim 18, wherein the first and second drive voltages are provided by a digital to analogue converter (DAC) which receives a 5 bit input derived from a 6 bit data signal (45) by dividing the 6 bit data signal by 3 and providing a divisor and a remainder.

20. A method as claimed in claim 19, wherein the divisor determines the first drive voltage, and the remainder determines whether the first and second drive voltages are the same or are different.

21. A method as claimed in any one of claims 18 to 20, wherein a plurality of sub-rows (10a, 10b) of pixels are addressed in turn, each sub-row comprising respective display elements for each pixel.

22. A method as claimed in any one of claims 18 to 20, wherein a plurality of rows of pixels are addressed in turn, each row being addressed once to

address both display elements and a second time to readdress the second display element.

23. A method as claimed in claim 17, wherein charge sharing between the display elements is used to generate the intermediate grey level.

24. A method as claimed in claim 23, wherein the first and second drive voltages are provided by a digital to analogue converter, which receives a 5 bit input.

25. A method as claimed in any one of claims 17 to 24, wherein the drive voltages are provided from a column driver circuit integrated onto the active plate of the active matrix display.